REMARKS

Claims 1-20 are pending in the current application. Claims 1, 7, 10 and 20 are independent claims.

Improper Finality

Applicant respectfully submits that the finality of the Office Action mailed on June 16, 2006 is improper. MPEP § 706.07(a) states the following:

> Under present practice, second or any subsequent actions on the merits shall be final, **except** when the Examiner introduces a new ground of rejection that is neither necessitated by Applicant's amendment of the claims nor based on information submitted in an Information Disclosure Statement ... (see MPEP § 706.07(a))

The Examiner has issued a new 35 U.S.C. § 112, first paragraph, enablement rejection relating to independent claims 1 and 7, and, in particular, claim elements beginning as "a high-speed control circuit ..." and "a low-speed and low-power control circuit ...". The Examiner has also issued a new 35 U.S.C. § 112, first paragraph, enablement rejection relating to independent claims 10 and 20, and, in particular, claim elements beginning as "selecting a control circuit ...". However, each of the claim portions cited by the Examiner and newly rejected have **never been amended**.

Accordingly, Applicant respectfully submits that the amendments previously made by Applicant to independent claims 1 and 7 have not necessitated the 35 U.S.C. § 112, first paragraph, enablement rejection because the amendments do not affect the portions of the claims now rejected (and even assuming they did, the enablement rejection of independent claims 1 and 10, which have never been amended would be sufficient to support improper finality). Further, the Applicant has filed no IDS which could possibly be said to necessitate the 35 U.S.C. § 112, first paragraph, enablement rejection, because the rejection is based entirely upon information within the specification as originally filed.

Accordingly, Applicant respectfully requests that the Examiner withdraw finality pursuant to MPEP § 706.07(d).

Allowable Subject Matter

Applicant notes that the Examiner has amended the 35 U.S.C. § 103(a) rejection to reject claims 1-2, 5-8, 10-11 and 15-20 instead of rejecting all of claims 1-20. However, the Examiner has not indicated that claims 3-4, 9 and 12-14 are allowable. Accordingly, Applicant respectfully requests that the Examiner properly indicate that claims 3-4, 9 and 12-14, which no longer appear to be rejected, would at least be allowable if rewritten into independent form.

Rejections under 35 U.S.C. § 112, First Paragraph

Claims 1-20 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicant respectfully traverses this art grounds of rejection.

The Examiner appears to be misinterpreting the claims by narrowly construing the term "in response" to mean "in **direct** response". However, this is **not** what the claim language recites. Independent claim 1 recites "a high-speed control circuit for controlling high-speed operations of at least one of the processor core and the peripheral device **in response** to the selection signal" (Emphasis added). As noted by the Examiner, the specification describes an example embodiment wherein a MUX 250 may select between connecting a low-speed and low-power control circuit and a high-speed control circuit with a processor core. Accordingly, in an example, if the MUX 250 receives a selection signal selecting the high-speed control circuit, the high-speed control circuit controls "at least one of the processor core and the peripheral device in response to the selection signal". Nowhere does independent claim 1 recite that the high-speed control circuit directly receives the selection signal, but rather, independent claim merely indicates that the selection signal,

either directly or indirectly, may determine whether the high-speed control circuit affects an operation of the processor core and/or the peripheral device. The above reasoning applies equally to the "low-speed and low-power control circuit".

Applicant respectfully submits that it is an improper claim interpretation to read the well-known language of "in response" to interpret as "in direct response". Accordingly, the Examiner's statement that "[i]t is uncertain how the selection signal directly controls the high-speed control circuit and the low-speed control circuit" is irrelevant because such a "direct" control need not be shown.

Claims 10 and 20 stand rejected for reasons similar to those already described. Here, the Examiner cannot understand how a selection circuit may select between control circuits. However, as already described, a selection circuit (e.g., a multiplexer) receives a selection signal and selects one of the plurality of inputs. Accordingly, if those plurality of inputs are received from a plurality of control circuits, one of ordinary skill in the art will clearly be able to understand how "selecting a control circuit from a plurality of control circuits" may be performed.

Further, Applicant reminds the Examiner that the Examiner is required to give the claims their broadest, reasonable interpretation. Applicant respectfully submits that it is entirely reasonable to construe "in response" so as to include direct and/or indirect responses.

Applicant respectfully requests that the Examiner withdraw this rejection.

Rejections under 35 U.S.C. § 103(a) – Kim in View of Dai and in Further View of Applicant's Admission of Prior Art (AAPA)

Claims 1-2, 5-8, 10-11 and 15-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim, U.S. Patent Application 2002/0026596 (hereinafter "Kim"), in view of Dai, U.S. Patent Application No. 2002/0083356 (hereinafter "Dai") and further in view of Applicant's Admission of Prior Art (AAPA).

Claims 1 and 7

Deficiencies of Kim

Kim is directed to a circuit and method of generating clock signals for a low power consumption CDMA modem chip design. In particular, Kim discloses a second clock generator 120 outputting a lower frequency clock signal CLOCK2 to a multiplexer 160 (e.g., see Figure 2 of Kim). The multiplexer 160 also receives a clock signal CLOCK1 at a higher frequency than the clock signal clock 2. The multiplexer 160 receives a clock selection signal from a clock selection unit 140. The selection signal received from the clock selection unit 140 is based on instructions received from a first clock controller 130. Claim 1 recites "a low-speed and low-power control circuit for controlling ... in response to the selection signal". The Examiner appears to read the claimed "low-speed and low-power control circuit" on the second clock generator 120 illustrated in Figure 2 of Kim.

Applicant's statement in the Amendment of March 29, 2006 that "the second clock generator 120 of Kim does not receive any selection signal from the first clock controller 130 and/or the clock selection unit 140" was not intended to imply that the selection signal need be directly received to be read upon by the claims, but was merely intended to point out a particular deficiency of Kim.

Applicant further agrees with the Examiner in that Kim:

> does not teach that the selecting circuit determines the operational state of the processor and outputs the selection signal based on the evaluation of the operational state of the processor. Additionally, Kim does not teach that the processor has a processor core and at least one peripheral device
>
> (see page 4 of the Office Action).

The Examiner seeks to combine Dai and the AAPA with Kim in order to overcome the above-described deficiencies of Kim. The Examiner alleges that Dai discloses "selecting

circuit [which] compares the operating frequency of the processor with a predetermined threshold frequency and outputs the selection signal based on the result" (page 5 of the Office Action) substantially in the Abstract lines 1-5 and paragraph [0013], lines 5-10 of Dai. Applicant respectfully disagrees.

Dai selects between operational states based only on a power source, not a processor characteristic

Initially, it appears that the Examiner has ignored, or at least not commented on, Applicant's remarks relating to the deficiencies of Dai filed in the Amendment of March 29, 2006. Accordingly, Applicant has resubmitted these arguments below, and respectfully requests that the Examiner carefully consider the below remarks.

Dai is directed to a method and apparatus to enhance processor power management. In particular, Dai discloses two operational states: a high performance state and a low power state. Dai associates that each of the two states are associated with predetermined core clock frequencies and supply voltage levels (see Abstract of Dai). However, the operating frequency of the processor of Dai is not compared with any threshold to determine whether or not to output a selection signal. **The only determining factor with regard to which state the Dai processor is operating in accordance with appears to be whether the system is powered with an external power source or an internal battery** (see paragraph [0013] of Dai). A review of Dai reveals that Dai does not disclose or suggest comparing an operating frequency of a processor with a threshold frequency to determine whether or not to output a selection signal for controlling an operation of the processor. Accordingly, the Examiner appears to be incorrect in asserting that "[d]epending on the processor frequency, the system

may be selected to perform in high performance mode or low power mode" (see page 5 of the Office Action). **Rather, the processor frequency appears to have nothing to do with the operating mode selection.**

The Examiner then further seeks to combine the AAPA with Kim and Dai to overcome the deficiencies of Kim and Dai. However, a cursory review of the AAPA reveals that the AAPA is similarly deficient in disclosing or suggesting the above-described deficiencies of the combination of Kim and Dai.

In view of the above remarks, Applicant respectfully submits that the combination of Kim, Dai and the AAPA cannot disclose or suggest "a selecting circuit for determining an operational state of the processor and for outputting a selection signal based on the determination" and "controlling high speed operations" and/or "low speed and low power operations" "in response to the selection signal" as recited in independent claim 1 and similarly recited in independent claim 7.

As such, claims 2, and 5-6 and 8, dependent upon independent claims 1 and 7, respectively, are likewise allowable over the combination of Kim, Dai and the AAPA for at least the reasons given above with respect to independent claims 1 and 7.

Claims 10 and 20

With respect to independent claims 10 and 20, the Examiner appears to reject each of claims 10 and 20 solely based on Kim and omits any reference to either Dai and/or the AAPA. Accordingly, Applicant will address the response to the rejections of claims 10 and 20 as if claims 10 and 20 were rejected based on Kim under 35 U.S.C. § 102.

As presently amended, Claim 10 is directed to a processor including "a circuit for selecting a control circuit from a plurality of control circuits based on an operational state or

operating frequency of a processor, the control circuit for controlling one of at least a first device and a second device" and claim 20 is directed to "selecting a control circuit from a plurality of control circuits based on an operational state or operating frequency of a processor".

Applicant has shown above how neither of Kim, Dai nor the AAPA disclose or suggest the presently amended claim limitation present in each of independent claims 1 and 20. Accordingly, Applicant respectfully submits that independent claims 1 and 20 are allowable over any combination of Kim, Dai and/or the AAPA.

As such, claims 11-19, depend upon independent claim 10, are likewise allowable over the combination of Kim, Dai and the AAPA for at least the reasons given above with respect to independent claim 10.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-20 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for

any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____

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